IN THE CLAIMS

Claim 1 (original): A method of converting an analog signal to accurate output digital codes of N-bits each, said method being performed in an analog to digital converter (ADC), said method comprising:

receiving said analog signal;

converting a sample of said analog signal into a N-bit digital code;

generating a difference voltage of said sample and a voltage level represented by said N-bit digital code;

converting said difference voltage into a P-bit digital code, wherein P is less than N; and

determining an accurate output digital code from said N-bit digital code and said P-bit digital code.

Claim 2 (original): The method of claim 1, further comprising:

generating said difference voltage at a plurality of time points;

performing said converting said difference voltage a corresponding number of times to generate a corresponding plurality of P-bit digital codes;

determining an average of said plurality of P-bit digital codes; and

performing an addition operation based on said average and said N-bit digital code to generate said accurate output digital code.

Claim 3 (original): The method of claim 2, wherein said difference voltage changes due to internal noise in said ADC and said addition operation reduces the effect of said internal noise in the value generated for said accurate output digital code.

Claim 4 (original): The method of claim 3, wherein said P is substantially smaller than said N, and equals an integer not less than [$\log_2$ (6 * σtot)], wherein * represents a multiplication operation, and Φtot represents a total of said internal noise.

Claim 5 (original): The method of claim 2, wherein said addition operation corrects said N-bit digital code in either positive direction or negative direction according to said P-bit digital code.

Claim 6 (currently amended): <u>A method of converting an analog signal to accurate output digital codes of N-bits each, said method being performed in an analog to digital converter (ADC), said method comprising:</u>

<u>receiving said analog signal;</u>

<u>converting a sample of said analog signal into a N-bit digital code;</u>

<u>generating a difference voltage of said sample and a voltage level represented by said N-bit digital code;</u>

<u>converting said difference voltage into a P-bit digital code, wherein P is less than N; and</u>

determining an accurate output digital code from said N-bit digital code and said P-bit digital code.

~~The method of claim 5,~~ wherein said ADC comprises N first set of capacitors and P second set of capacitors, wherein said first set of capacitors are operated according to successive approximation principle (SAP) to determine said N bit digital code, and said second set of capacitors are thereafter operated according to said SAP to determine said P-bit digital code, said method further comprising:

sampling said sample on said first set of capacitors in a sampling phase, wherein said sampling is performed before converting said sample into said N-bit digital code;

connecting a first capacitor contained in said second set of capacitors to a Vref voltage and the remaining ones of said second set of capacitors to ground in said sampling phase, wherein said first capacitor corresponds to a most significant bit (MSB) of said P-bit digital code;

adding all but the MSB of said P-bit digital code to said N-bit digital code if the MSB of said P-bit digital code is of one logical value; and

subtracting all but the MSB of said P-bit digital code from said N-bit digital code if the MSB of said P-bit digital code is of the other logical value.

Claim 7 (currently amended): A successive approximation type analog to digital converter (SAR ADC) converting a sample of an input analog signal into an accurate N-bit digital code, said SAR ADC comprising:

a comparator providing a comparison result of a first analog signal and said sample;

a digital to analog converter (DAC) receiving an intermediate N-bit value and an intermediate P-bit value, said DAC generating said first analog signal based on said intermediate N-bit value and said intermediate P-bit value; and

a SAR logic determining a first N-bit digital code according to successive approximation principle (SAP) by sending said intermediate N-bit value in each of N iterations, said SAR logic then generating a first P-bit digital code according to said SAP by sending said intermediate P-bit value in each of P iterations, wherein said first N-bit digital code is corrected using said first P-bit digital code to generate said accurate N-bit digital code wherein P is less than N.

Claim 8 (currently amended): A successive approximation type analog to digital converter (SAR ADC) converting a sample of an input analog signal into an accurate N-bit digital code, said SAR ADC comprising:

a comparator providing a comparison result of a first analog signal and said sample;

a digital to analog converter (DAC) receiving an intermediate N-bit value and an intermediate P-bit value, said DAC generating said first analog signal based on said intermediate N-bit value and said intermediate P-bit value; and

a SAR logic determining a first N-bit digital code according to successive approximation principle (SAP) by sending said intermediate N-bit value in each of N iterations, said SAR logic then generating a first P-bit digital code according to said

SAP by sending said intermediate P-bit value in each of P iterations, wherein said first N-bit digital code is corrected using said first P-bit digital code to generate said accurate N-bit digital code.

~~The SAR ADC of claim 7,~~ wherein said SAR logic determines a plurality of P-bit digital codes including said first P-bit digital code, said plurality of P-bit digital codes being averaged to generate an average value, wherein said first N-bit digital code is corrected using said average value.

Claim 9 (original): The SAR ADC of claim 8, wherein said DAC comprises:

N first set of capacitors, each having a capacitance value corresponding to a weight of a corresponding one of a N-bit code;

N first set of switches, wherein each of said first set of switches connects a corresponding one of said first set of capacitors to said sample in a sampling phase of said SAP, each of said first set of switches connecting a corresponding one of said first set of capacitors to a ground or a reference voltage according to a corresponding bit of said intermediate N-bit value in a conversion phase of said SAP;

P second set of capacitors, each having a capacitance value corresponding to a weight of a corresponding one of a P-bit code, wherein P is less than N; and

P second set of switches, each of said second set of switches connecting a corresponding one of said second set of capacitors to a ground or a reference voltage according to a corresponding bit of said intermediate P-bit value.

Claim 10 (original): The SAR ADC of claim 9, wherein another end of each of said first set of capacitors and said second set of capacitors is connected to a V_{mid} voltage by a third switch, wherein said third switch is in a closed state in said sampling phase and in an open state in said conversion phase, wherein an intermediate analog signal equaling the following voltage is generated by said DAC:

$$V_{top}=V_{mid}-V_{inp}+\sum_{i=1}^{N} b_i \frac{V_{ref}}{2^i}+\sum_{j=1}^{P} b_j \frac{V_{ref}}{2^j}$$

wherein V_{ref} and V_{inp} represent said reference voltage and voltage of said sample, and b_i represents the i^{th} bit of said intermediate N-bit value and b_j represents the j^{th} bit of said intermediate P-bit value.

Claim 11 (original): The SAR ADC of claim 10, wherein said comparator compares said intermediate analog signal with said V_{mid} voltage to generate said comparison result.

Claim 12 (original): The SAR ADC of claim 11, wherein said average value is used to correct said first N-bit digital code in either positive or negative direction.

Claim 13 (original): The SAR ADC of claim 12, wherein SAR logic sets a most significant bit (MSB) of said P-bit digital code to one in said sampling phase, and adds all but the MSB of said average value to said N-bit digital code if the MSB of said average value is of one logical value, said SAR logic subtracting all but the

MSB of said average value from said N-bit digital code if the MSB of said P-bit digital code is of the other logical value.

Claim 14 (original): The SAR ADC of claim 13, wherein said DAC comprises more than P of said second set of switches, and wherein P is determined by a noise introduced internally in said SAR ADC.

Claim 15 (original): The SAR ADC of claim 13, wherein said noise comprises components introduced by said DAC and said comparator.

Claim 16 (original): A successive approximation type analog to digital converter (SAR ADC) converting an analog signal to accurate output digital codes of N-bits each, said SAR ADC comprising:

means for receiving said analog signal;

means for converting a sample of said analog signal into a N-bit digital code;

means for generating a difference voltage of said sample and a voltage level represented by said N-bit digital code;

means for converting said difference voltage into a P-bit digital code, wherein P is less than N; and

means for determining an accurate output digital code from said N-bit digital code and said P-bit digital code.

Claim 17 (original): The SAR ADC of claim 16, further comprising:

means for generating said difference voltage at a plurality of time points, wherein said means for converting said difference voltage converts said difference voltage a corresponding number of times to generate a corresponding plurality of P-bit digital codes;

means for determining an average of said plurality of P-bit digital codes; and

means for performing an addition operation based on said average and said N-bit digital code to generate said accurate output digital code.

Claim 18 (original): The SAR ADC of claim 17, wherein said difference voltage changes due to internal noise in said SAR ADC and said addition operation reduces the effect of said internal noise in the value generated for said accurate output digital code.

Claim 19 (currently amended): <u>A successive approximation type analog to digital converter (SAR ADC) converting an analog signal to accurate output digital codes of N-bits each, said SAR ADC comprising:</u>

<u>means for receiving said analog signal;</u>

<u>means for converting a sample of said analog signal into a N-bit digital code;</u>

<u>means for generating a difference voltage of said sample and a voltage level represented by said N-bit digital code;</u>

<u>means for converting said difference voltage into a P-bit digital code, wherein P is less than N; and</u>

means for determining an accurate output digital code from said N-bit digital code and said P-bit digital code,

~~The SAR ADC of claim 18,~~ wherein said P is substantially smaller than said N, and equals an integer not less than [$\log_2(6 * \sigma tot)$], wherein * represents a multiplication operation, and Φtot represents a total of said internal noise.

Claim 20 (currently amended): A successive approximation type analog to digital converter (SAR ADC) converting an analog signal to accurate output digital codes of N-bits each, said SAR ADC comprising:

means for receiving said analog signal;

means for converting a sample of said analog signal into a N-bit digital code;

means for generating a difference voltage of said sample and a voltage level represented by said N-bit digital code;

means for converting said difference voltage into a P-bit digital code, wherein P is less than N;

means for determining an accurate output digital code from said N-bit digital code and said P-bit digital code,

means for generating said difference voltage at a plurality of time points, wherein said means for converting said difference voltage converts said difference voltage a corresponding number of times to generate a corresponding plurality of P-bit digital codes;

means for determining an average of said plurality of P-bit digital codes; and

means for performing an addition operation based on said average and said N-bit digital code to generate said accurate output digital code.

~~The SAR ADC of claim 17,~~ wherein said addition operation corrects said N-bit digital code in either positive direction or negative direction according to said P-bit digital code.

Claim 21 (original): The SAR ADC of claim 20, wherein said means for converting a sample comprises N first set of capacitors and P second set of capacitors, wherein said first set of capacitors are operated according to successive approximation principle (SAP) to determine said N bit digital code, and said second set of capacitors are thereafter operated according to said SAP to determine said P-bit digital code, said SAR ADC further comprising:

means for sampling said sample on said first set of capacitors in a sampling phase, wherein said means for sampling is performed before converting said sample into said N-bit digital code;

means for connecting a first capacitor contained in said second set of capacitors to a Vref voltage and the remaining ones of said second set of capacitors to ground in said sampling phase, wherein said first capacitor corresponds to a most significant bit (MSB) of said P-bit digital code;

means for adding all but the MSB of said P-bit digital code to said N-bit digital code if the MSB of said P-bit digital code is of one logical value; and

means for subtracting all but the MSB of said P-bit digital code from said N-bit digital code if the MSB of said P-bit digital code is of the other logical value.

Claim 22 (currently amended): A system comprising:

an analog processor processing an analog signal to generate an analog sample;

a successive approximation type analog to digital converter (SAR ADC) converting said analog sample into an accurate N-bit digital code, said SAR ADC comprising:

a comparator providing a comparison result of a first analog signal and said sample;

a digital to analog converter (DAC) receiving an intermediate N-bit value and an intermediate P-bit value, said DAC generating said first analog signal based on said intermediate N-bit value and said intermediate P-bit value; and

a SAR logic determining a first N-bit digital code according to successive approximation principle (SAP) by sending said intermediate N-bit value in each of N iterations, said SAR logic then generating a first P-bit digital code according to said SAP by sending said intermediate P-bit value in each of P iterations, wherein said first N-bit digital code is corrected using said first P-bit digital code to generate said accurate N-bit digital code; and

a processing unit receiving said accurate output digital code <u>wherein P is less than N</u>.

Claim 23 (original): The system of claim 22, wherein said SAR logic determines a plurality of P-bit digital codes including said first P-bit digital code, said plurality of P-bit digital codes being averaged to generate an average value, wherein said first N-bit digital code is corrected using said average value.

Claim 24 (currently amended): A system comprising:

an analog processor processing an analog signal to generate an analog sample;

a successive approximation type analog to digital converter (SAR ADC) converting said analog sample into an accurate N-bit digital code, said SAR ADC comprising:

a comparator providing a comparison result of a first analog signal and said sample;

a digital to analog converter (DAC) receiving an intermediate N-bit value and an intermediate P-bit value, said DAC generating said first analog signal based on said intermediate N-bit value and said intermediate P-bit value; and

a SAR logic determining a first N-bit digital code according to successive approximation principle (SAP) by sending said intermediate N-bit value in each of N iterations, said SAR logic then generating a first P-bit digital code according to said SAP by sending said intermediate P-bit value in each of P iterations, wherein said first N-bit

digital code is corrected using said first P-bit digital code to generate said accurate N-bit digital code; and

a processing unit receiving said accurate output digital code.

~~The system of claim 23,~~ wherein said DAC comprises:

N first set of capacitors, each having a capacitance value corresponding to a weight of a corresponding one of a N-bit code;

N first set of switches, wherein each of said first set of switches connects a corresponding one of said first set of capacitors to said sample in a sampling phase of said SAP, each of said first set of switches connecting a corresponding one of said first set of capacitors to a ground or a reference voltage according to a corresponding bit of said intermediate N-bit value in a conversion phase of said SAP;

P second set of capacitors, each having a capacitance value corresponding to a weight of a corresponding one of a P-bit code, wherein P is less than N; and

P second set of switches, each of said second set of switches connecting a corresponding one of said second set of capacitors to a ground or a reference voltage according to a corresponding bit of said intermediate P-bit value.

Claim 25 (original): The system of claim 24, wherein another end of each of said first set of capacitors and said second set of capacitors is connected to a V_{mid} voltage by a third switch, wherein said third switch is in a closed state in said sampling phase and in an open state in said conversion phase, wherein an intermediate analog signal equaling the following voltage is generated by said DAC:

$$V_{top} = V_{mid} - V_{inp} + \sum_{i=1}^{N} b_i \frac{V_{ref}}{2^i} + \sum_{j=1}^{P} b_j \frac{V_{ref}}{2^j}$$

wherein V_{ref} and V_{inp} represent said reference voltage and voltage of said sample, and b_i represents the i^{th} bit of said intermediate N-bit value and b_j represents the j^{th} bit of said intermediate P-bit value.

Claim 26 (original): The system of claim 25, wherein said comparator compares said intermediate analog signal with said V_{mid} voltage to generate said comparison result.

Claim 27 (original): The system of claim 26, wherein said average value is used to correct said first N-bit digital code in either positive or negative direction.

Claim 28 (original): The system of claim 27, wherein SAR logic sets a most significant bit (MSB) of said P-bit digital code to one in said sampling phase, and adds all but the MSB of said average value to said N-bit digital code if the MSB of said average value is of one logical value, said SAR logic subtracting all but the MSB of said average value from said N-bit digital code if the MSB of said P-bit digital code is of the other logical value.

Claim 29 (original): The system of claim 28, wherein said DAC comprises more than P of said second set of switches, and wherein P is determined by a noise introduced internally in said SAR ADC.

Claim 30 (original): The system of claim 28, wherein said noise comprises components introduced by said DAC and said comparator.

Claim 31 (original): The system of claim 30, wherein said system comprises a global positioning system receiver, said system further comprising an antenna to receive said analog signal and provide to said analog processor.